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(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **ALBA PINTO**, Carlos, A. [PE/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **SETHURAMAN, Ramanathan** [IN/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **SRINIVASAN, Balakrishnan** [IN/NL]; c/o Prof. Holstlaan 6,

NL-5656 AA Eindhoven (NL). **PETERS, Harm, J., A.**, M. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **PESET LLOPIS, Rafael** [ES/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

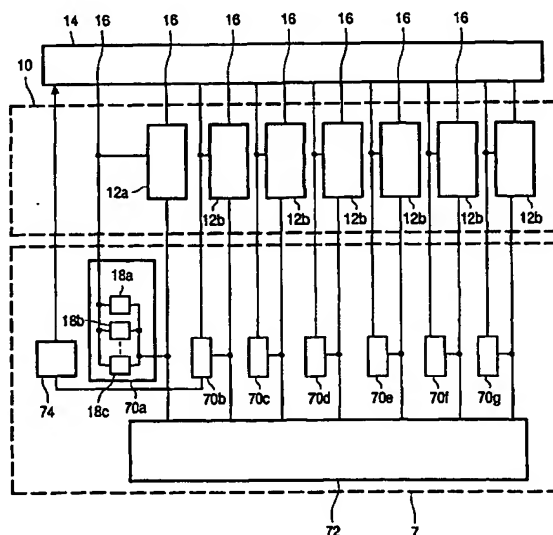
(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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(54) Title: **VLIW PROCESSOR WITH POWER SAVING**



(57) Abstract: A data processing apparatus has an instruction memory system arranged to output an instruction word, capable of containing a plurality of instructions, respective instruction words being output in response to respective instruction addresses. An instruction execution unit contains a plurality of functional units, each capable of executing a respective instruction from the instruction word in parallel with execution of other instructions from the instruction word by other ones of the functional units. A power saving circuit is provided to switch a selectable subset of the functional units and/or parts of the instruction memory to a power saving state, while other functional units and parts of the instruction memory continue processing instructions in a normal power consuming state. The power saving circuit selects the functional units and/or parts of the instruction memory dependent on program execution.

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